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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,066	06/24/2003	Satoshi Matsuda	008312-0304355	1198

909 7590 11/30/2005

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/602,066	MATSUDA ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,6,8,10 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,6,8,10 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/101,950.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2, 5, 6, 8, 10 and 22-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, lines 5-6, 21, claim 10, lines 6-7, 18, the phrase "that portion of said semiconductor substrate" is unclear as to what portion is it being referred to. Is it meant "a portion of said semiconductor substrate"?

Claim 8, lines 2-3, the phrase "an upper surface of said interlayer insulating film being substantially equal to an upper surface of said gate electrode" is vague and indefinite. Fig. 6 discloses an upper surface of said interlayer insulating film [209] being coplanar to an upper surface of said gate electrode [207]. Therefore, the phrase should rewrite as "an upper surface of said interlayer insulating film being coplanar to an upper surface of said gate electrode".

Claim 22, lines 1-2, claim 23, lines 1-2, the phrase "the lower end of the gate electrode is cut out" is unclear as to what is it meant. Is it meant the right or left region outside the protruding portion at the bottom of the gate electrode?

Claim 23, line 3, the phrase "the second gate insulating film" is unclear as to where is the second gate insulating film in the device.

2. Claims 8 and 10 are objected to because of the following informalities: Claim 8, lines 2-3, the phrase "said gate side wall insulating film" has no antecedent basis. Claim 10, lines 20-21, the phrase "the conductivity type of said semiconductor substrate" has no antecedent basis. Appropriate correction is required.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 5, 6, 8, 22 and 24 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo in view of Shell et al.

In regards to claim 2, Maruo discloses a semiconductor device in fig. 1. It comprising: (a) a semiconductor substrate [10]; (b) a pair of first diffusion layers [17, 18, 18a] formed within said semiconductor substrate; (c) a gate insulating film [14, 15] including: (i) a first insulating film portion [14] formed on that portion of said semiconductor substrate which is positioned between said first diffusion layers [17, 18, 18a], and (ii) a second insulating film portion [15] positioned on both edges of said first insulating film portion, said second insulating film portion having a thickness that is larger than a thickness of said first insulating film portion; (d) a gate electrode [16] having a first gate portion formed on the first insulating film portion and a second gate portion formed on the second insulating film portion, in which the first and second gate portions are formed of the same material (polysilicon); (e) a first gate side wall insulating film (a portion of the insulating film [23] extends from the upper right hand corner of the electrode [16] to the lower right hand corner of layer [23]) formed on a side surface of said gate electrode and on a side surface of said second insulating film portion, the first gate side wall insulating film having a first side surface and a second side surface, the

first gate side surface being opposite to a side surface facing the gate electrode, the second side surface being opposite to a side surface facing the second insulating film portion, the first side surface being flush with the second side surface.

Maruo differs from the claimed invention by not showing a second diffusion layer formed apart from said first diffusion layers within that portion of said semiconductor substrate which is positioned below said first insulating film portion.

Shell et al. disclose a second diffusion layer [40] formed apart from said first diffusion layers [60, 62] within that portion of said semiconductor substrate [10], which is positioned below said first insulating film portion [20] in fig. 9. Shell et al. further disclose the self-aligned anti-punchthrough implant channels can be formed in the N^- doped substrates for the P-channel FETs by reversing the dopant polarity (i.e., [40] is n-type in a P-channel FET) (col. 7, lines 11-14).

Since both Maruo and Shell et al. teach a LDD-type p-channel MOSFET, it would have been obvious to have the n-type implant of Shell et al. in Maruo because it prevents punchthrough in the channel region.

In regards to claim 5, Maruo further discloses said first diffusion layers further comprises: a pair of extension regions [17] formed below said gate side wall insulating film apart from said second diffusion layer; and a pair of source-drain regions [18, 18a] formed in contact with said extension regions on a side opposite said second diffusion layer.

In regards to claim 6, Maruo further discloses further a second gate side wall insulating film (a portion of the layer [23] extends from the upper right hand corner of the

gate [16] to a middle side portion of layer [25a]) formed on a side surface of the first gate side wall insulating film.

In regards to claim 8, Maruo further discloses an interlayer insulating film [23] formed to surround a portion of said gate side wall insulating film, an upper surface of said interlayer insulating film (a portion of layer [23] that has an upper surface coplanar to an upper surface of gate [16]) being substantially equal to an upper surface of said gate electrode.

In regards to claim 22, Maruo further discloses the lower end of the gate electrode [16] is cut out (a right or left region outside the bottom protruding portion of gate layer [16]), and a cut out region of the lower end of the gate electrode is embedded with only the second insulating film portion [15].

In regards to claim 24, Maruo further discloses an upper surface of the second insulating film portion [15] is positioned higher than a top surface of the first insulating film portion [14], and a bottom surface of the second insulating film portion [15] is positioned lower than a bottom surface of the first insulating film portion [14].

5. Applicant's arguments with respect to claims 2, 5, 6 and 8 have been considered but are moot in view of the new ground(s) of rejection.

6. Claim 10 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
November 27, 2005

Steven Loke